Development of a high-speed digital pulse signal acquisition and processing system based on MTCA for liquid scintillator neutron detector on EAST

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Abstract: In this experimental study, involving deuterium–deuterium fusion neutron emission spectroscopy (NES) measurement on the experimental advanced superconducting tokamak (EAST), a liquid scintillator detector (BC501A) was employed. This decision was based on the detector's superior sensitivity, optimal time-response, and its exceptional n-γ discrimination capability. This detector emits fast pulse signals that are as narrow as 100 ns, with high count rates that can peak at several Mcps. However, conventional nuclear circuits faced challenges in performing pulse height analysis, n–γ pulse shape discrimination (PSD), and in recording the entire pulse waveform under such high-count-rate conditions. To address these challenges, a high-speed digital pulse signal acquisition and processing system was designed. The system was developed around a micro-telecommunications computing architecture (MTCA). Within this structure, a signal acquisition and processing (SAQP) module communicated through PCI Express (PCIe) links, achieving a bandwidth of up to 1.6 GB/s. To accurately capture the detailed shape of the pulses, four channels of analog-to-digital converters (ADCs) were used, each with a 500-MSPS sampling rate and a 14-bit resolution, ensuring an accuracy that surpassed 11 bits. An n-γ discrimination algorithm, based on the two-gate integral method, was also developed. Implemented within field programmable gate arrays (FPGA), this algorithm provided a real-time n-

γ discrimination spectrum for pulse height analysis. The system underwent rigorous testing in a laboratory setting and during an EAST experiment. The results confirmed that the innovative SAQP system can satisfy the demanding requirements of high-parameter experiments, manage count rates of up to 2 Mcps, execute real-time n-γ discrimination algorithms, and record entire pulse waveforms without any data loss.

Key words: EAST, NES, High-speed, MTCA, n-γ discrimination, Entire pulse waveform

1 Introduction

Neutron emission spectroscopy (NES) is important in high-power thermonuclear fusion experiments. It can be used to evaluate the effectiveness of heating systems and provide information related to fuel ion composition, ion velocity distributions, and ion temperature [1-5]. The NES measurement on experimental advanced superconducting tokamak (EAST) adopts liquid scintillator detector (BC501A) due to its high sensitivity, excellent time-response and quality n-γ discrimination property [6-9].

The BC501A detector emits rapid pulse signals as narrow as 100 ns, necessitating the use of high-sampling-rate analog-to-digital converters (ADCs) to capture the intricate details of the pulses. This detector is sensitive to both neutrons and gamma radiation. During the start-up phase of discharge, runaway electrons emerge. A BC501A detector can identify the bremsstrahlung emission in the hard X-ray range produced by these runaway electrons [10]. When neutron beam injection (NBI) auxiliary heating systems are added to the plasma, intense neutron and gamma-ray emissions are produced owing to the reaction of the injected neutron beam ions with the main plasma [11-14]. Therefore, the count rate of the NES system significantly increases, exceeding 1 Mcps, during the start-up phase of the discharge or under the NBI heating scenario. It is crucial to record the entire pulse waveform, as it offers comprehensive data support for subsequent offline data processing. This aids in interpreting the underlying physics, enabling activities like pile-up pulse reconstruction, noise reduction, and enhancement

of energy resolution. Given these considerations, the pivotal requirements for the NES system include high acquisition rates (reaching hundreds of mega samples per second), a substantial physical event rate (up to several million events per second), the capability to document vast amounts of data, and the execution of real-time pulse processing algorithms, such as n-γ discrimination.

The current signal acquisition and processing (SAQP) system for NES on EAST utilizes the commercial CAEN VX1730D product. This VX1730D digitizer boasts eight analog input channels and operates using the proprietary CAEN CONET protocol, offering a transfer rate of 80MB/s. At present, all eight input channels connect to various neutron detectors to capture diagnostic data, such as neutron flux and neutron emission spectroscopy. Nonetheless, this system encounters data loss at elevated count rates and can't consistently record entire pulse waveforms due to its limited transfer bandwidth. Such limitations hinder the NES system's efficacy in high-parameter plasma experiments. Additionally, two neighboring channels must have matching pulse record lengths, causing certain detector output signals to not be recorded at the optimal length. In contrast, the SAQP systems in the International Thermonuclear Experimental Reactor (ITER) radial neutron camera, Joint European Torus (JET) gamma-ray camera, and JET gamma-ray spectrometer are capable of executing intricate real-time algorithms, like pulse height analysis and n-γ discrimination. They can also record full pulse waveforms at impressive count rates of 2 Mcps [15-18]. Thus, there is a pressing need to develop a new SAQP system for the EAST NES.

Micro telecommunications computing architecture (MTCA) control and data acquisition instrumentation, with excellent data transfer rate, channel density, and high-availability characteristics, have fostered several applications in fusion control and diagnostics [19-22]. In this study, an MTCA-based high-speed digital pulse SAQP system was devised. Paired with a BC501A liquid scintillator detector located at the H-port of the EAST, this combination formed the NES system. The SAQP system boasts several features: (a) It has four channels with a 500 MSPS sampling rate and a 14-bit resolution, maintaining accuracy above 11 bits. These analog-to-digital converters (ADCs) are essential to capture the intricate details of the pulses; (b) Interconnecting

through PCI Express (PCIe) links with direct memory access (DMA), the system achieves a bandwidth up to 1.6 GB/s. Consequently, the SAQP system can record the entire pulse waveform due to this robust transfer rate; (c) An n-γ discrimination algorithm, based on the two-gate integral method, was formulated and integrated into field programmable gate arrays (FPGA). This setup provides a real-time n-γ discrimination spectrum for pulse height analysis; (d) The system's four analog input channels can be individually calibrated to different operating parameters. This flexibility ensures simultaneous data acquisition from detectors with varying signal widths. Ultimately, the goal of this newly-developed SAQP system is to ensure that the NES setup meets the stringent requirements of high-parameter experiments. It aims to accommodate a high-count-rate of 2 Mcps, execute real-time n-γ discrimination algorithms, and capture the entirety of the pulse waveform without any data loss.

2 Architecture design

The NES system used in the EAST consists of a collimator, BC501A detector, photomultiplier tube (PMT), and a SAQP system. The NES system must be shielded and collimated to reduce the impact of scattered neutrons and background gamma-rays on the detector output signal [23]. The BC501A detector, manufactured by Saint-Gobain, boasts an excellent n-γ discrimination capability. It offers high detection efficiency for fast neutrons and has a brief decay time. This makes it ideal for high-count-rate scenarios and particularly apt for detecting pulsed neutron radiation during EAST discharges. This detector was optically paired with a 2-in Hamamatsu R329-02 PMT. The negative voltage pulse signal, ranging between 0 and –2 V, emanating from the PMT anode was directly captured by the SAQP system after traveling through a shielded cable. To protect against radiation damage, the SAQP system was positioned in a neutron diagnostic laboratory, safeguarded by a radiation-shielding wall.

Designed around the MTCA framework, the SAQP system comprises an MTCA shelf, an MTCA Carrier Hub (MCH), a custom-developed Advanced Mezzanine Card (AMC) tailored for signal acquisition and processing (henceforth labeled the SAQP

module), a PCIe uplink module, an optical uplink cable, and a dedicated host computer. This setup is depicted in Fig. 1.

The MCH functions as the central controller, overseeing all AMC cards on the shelf. Within the MCH, the MTCA Carrier Management Controller (MCMC) supervises the power toggling and hot swapping of all AMC cards. This is achieved via the Intelligent Platform Management Bus (IPMB), and the system also continually monitors the hardware's health metrics. The specific MCH employed in this design was the NAT-MCH-PHYS80, a product of N. A. T. catering to the demand for greater bandwidth in both AMCs and optical uplinks within PCIe-based MTCA platforms, the NAT-MCH-PHYS80 features an 80-port PCIe Gen3 switch. This permits each of the 12 AMCs in an MTCA system to establish a connection through an x4-PCIe-link [24]. Moreover, it facilitates an x8 optical PCIe uplink to external high-performance servers and additional MTCA systems. An x8-PCIe-link between the NAT-MCH-PHYS80 and the host computer was created using a PCIe uplink module and an optical uplink cable.

Describing the operational flow of the SAQP system: initially, the signal undergoes acquisition and processing by the SAQP module. The processed data are then relayed to the MCH via the backplane. Conclusively, the MCH forwards the data to the host computer for storage through the x8 optical PCIe uplink.
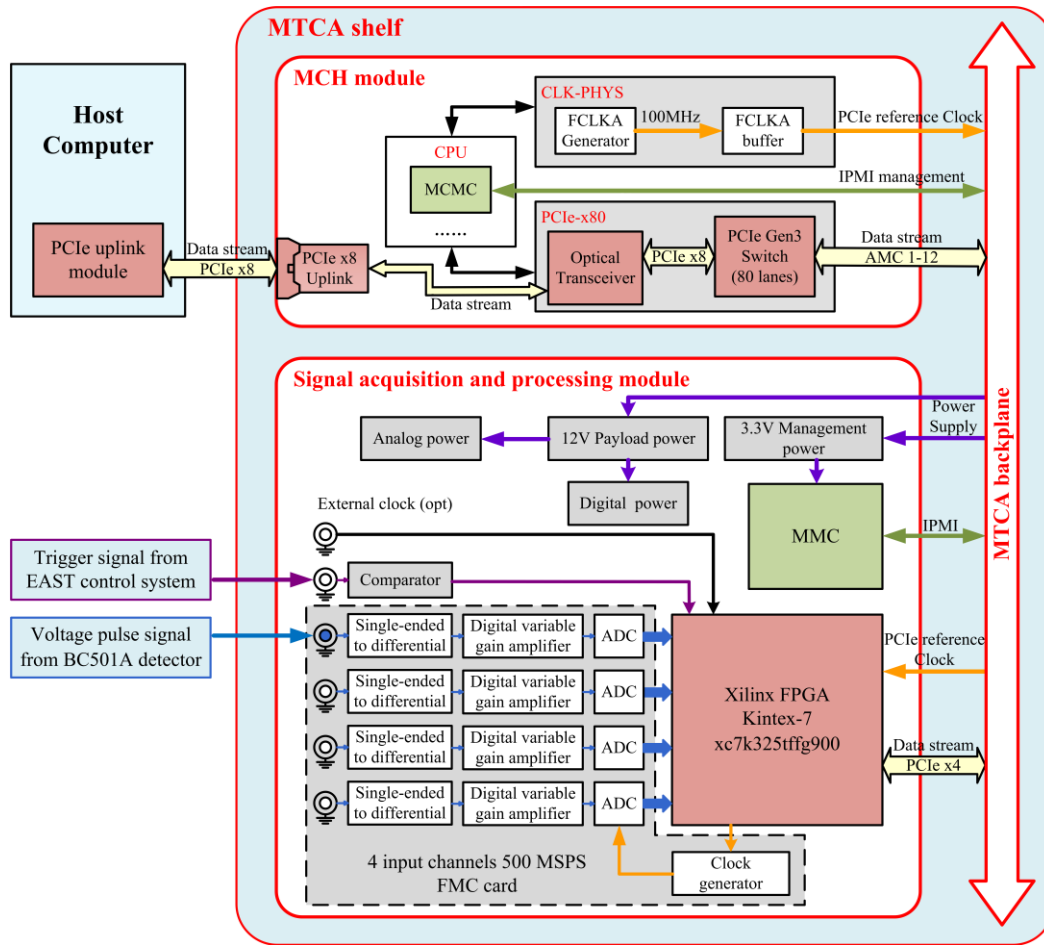
Fig. 1 Architecture of SAQP system based on MTCA used on NES system.

3 Hardware design of SAQP module

The SAQP module designed in this study is based on the Advanced Mezzanine Card^{TM} specifications [25]. The SAQP module was designed with a 4HP height and double width form factor, measuring 148.8×18.96×181.5 mm, to adequately accommodate the 4-channel ADCs. Fig. 1 displays a block diagram of the SAQP module. Incorporating a mother-daughter board structure, the SAQP module connects via an FMC connector, as depicted in Fig. 2. Based on its functions, the SAQP module can be categorized into a Module Management Controller (MMC) and a function module.
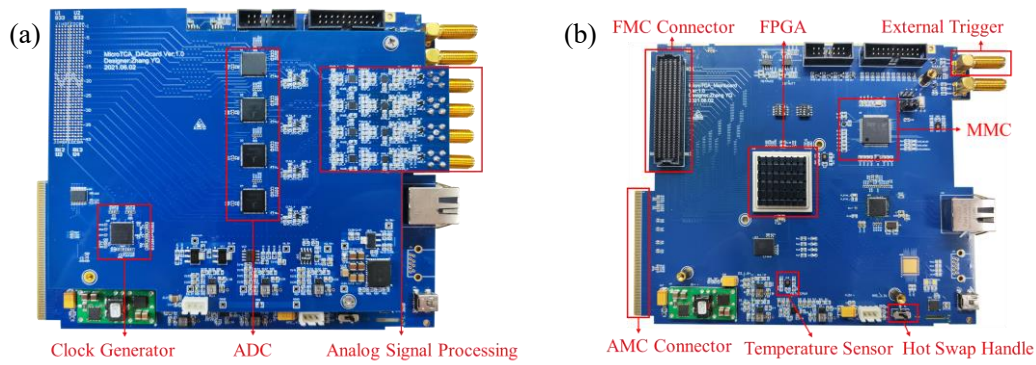
Fig. 2 Electronic design of SAQP module. (a) SAQP module. (b) Motherboard.

3.1 Hardware design of MMC

The MMC is the management and control unit on the SAQP module, which communicates with the MCH through the IPMB to implement Intelligent Platform Management Interface (IPMI) functions, such as module activation, power on/off, hot-swap, E-Keying, and temperature monitoring. MMC modules must be designed to be as compact as possible to reserve more area for function modules. Moreover, the MMC should not draw more than 150 mA from the management power according to the specification [25]. Considering the cost, size, and power consumption, the STM32F429VET6 was selected as the control chip for the MMC, which has a high main frequency (180 MHz), large memory (256 KB SRAM + 512 KB FLASH), low power consumption, and a compact package [26]. Two temperature sensors (HDC2080) were deployed on the SAQP module to collect the temperature information of the power supply and FPGA. A hot-swap handle on the motherboard is used to generate a hot-swap signal to indicate the insertion or extraction of the module. The MMC solution designed in this study has the features of small size and low power consumption (operating current of 15 mA) which can satisfy the above requirements.

3.2 Hardware design of function module

The function module consisted of an analog signal acquisition module, an external trigger module, a core processing module, and a bus interface.

The analog signal acquisition module is located on the daughter board, as shown in Fig. 2(a). The four input channels have a differential DC coupling, featuring an input range from –2 V to 3 V and a 50-ohm impedance match. The pulse signal is first channeled into the SAQP module via the SMA interface. Following this, the single-ended differential chip (LMH5401) transforms the input single-ended signal into a differential signal, which then serves as the input for the digital variable gain amplifier (LMH6401) [27]. The gain of the LMH6401 can be programmed to adjust the amplitude of the output signal to maximize the input dynamic range of the ADC, thereby improving its signal-to-noise ratio [28]. The signal was then fed into the ADC through an anti-aliasing filter module and converted into a digital signal.

Choosing the appropriate ADC sampling rate and bit resolution is crucial for enhancing energy resolution and n-γ discrimination. The BC501A detector emits pulse signals characterized by a pulse width of roughly 100 ns, a rise time of around 10 ns, and a Full Width Half Maximum (FWHM) of about 15 ns. Following a fast Fourier transform (FFT), the frequency spectrum composition of this waveform can extend up to 100 MHz. As per sampling theory, the sampling rate should exceed 250 MHz. Furthermore, the higher the ADC's sampling rate and bit resolution, the more precise the gate integration becomes, which is a vital metric for n-γ discrimination and energy estimation. However, the enhancement in precision becomes less noticeable once the sampling rate hits 500 MHz and the bit resolution approaches 11 bits [29]. Given the signal's narrow pulse width, rapid rise time, as previously described, and the demands for energy resolution and n-γ discrimination, the ISLA214P50 ADC boasting a 500-MSPS sampling rate and 14-bit resolution was chosen. This ADC processes an input analog signal into its digital counterpart through steps like sampling, quantization, and encoding. It then delivers the digital data in a double-data-rate format supported by a 250 MHz data output clock. The FPGA retrieves the ADC's output data utilizing double-edge (both rising and falling edges) sampling for subsequent algorithm analysis. Lastly, the high-performance LMK04828B clock conditioner chip from TI was picked to produce a 500 MHz ultra-low jitter clock, serving as the ADC's sampling clock.

The motherboard houses the external trigger module, bus interface, and core processing module, as depicted in Fig. 2(b). The external trigger module accepts the TTL hardware trigger signal dispatched by the EAST central control system, prompting the SAQP system to initiate operations promptly.

Given the demanding processing and transfer speed requirements at 250 MHz, only rapid-programmable devices are suitable. Thus, the Kintex-7 family (xc7k325tffg900) FPGA from Xilinx was chosen as the central processing unit for the function module. This FPGA is directly interfaced with four ADC channels and the bus interface, allowing for: (a) control over the digital variable gain amplifier (LMH6401) to refine signal amplitude, thus enhancing the signal-to-noise ratio; (b) management of the operational mode, encompassing both Acquisition and pulse shape discrimination (PSD) modes; (c) use as a temporary data buffer, housing ADC data for real-time data processing; (d) the execution of high-velocity algorithms, such as signal trigger detection and n-γ discrimination; (e) provision of a gigabit communication interface via the x4-PCIe Gen2 link.

The bus interface employs an AMC connector as outlined by the Advanced Mezzanine Card^{TM} standards. The AMC connector's interconnection interfaces are categorized into four functional units: (a) The Fabric Interface, purposed for high-speed data transmission and utilized here as an x4-PCIe data channel; (b) The System Management Interface, offering the IPMB bus to facilitate communication between the MMC and MCH; (c) The AMC Clock Interface, where the integrated clock generator within the MCH forwards a 100 MHz clock to the AMC board, serving as the PCIe reference clock; (d) The power/ground interface, supplying a 3.3 V management power for the MMC module and 12 V payload power for the function module

4 Firmware design

The firmware design included the STM32 firmware design for the MMC module and FPGA firmware design for the function module.

4.1 STM32 firmware design

In the MTCA system, application boards are referred to as AMC boards. These boards must incorporate an MMC, typically a microcontroller. The MMC's primary duties include monitoring the board's health and serving as a communication bridge between the MCMC and the application, facilitated through IPMI [30]. The NES-RTOS-MMC was developed based on openMMC, which is an open-source firmware designed for board management in MTCA systems.

The NES-RTOS-MMC operates atop FreeRTOS, enabling the application code to simultaneously execute multiple tasks using a single core. The NES-RTOS-MMC encompasses tasks such as the field-replaceable unit (FRU) information task, LED task, hot-swap task, temperature monitoring, tasks for sending and receiving IPMI instructions, and tasks to enable or disable the AMC board. In a typical module insertion process, the AMC board is first slotted into an available space in the MTCA shelf. Following this, the MCH provides management power to the MMC. At this juncture, the NES-RTOS-MMC sets up the FRU information, which encapsulates details like module current, clock interface, and direct connectivity. As the next step, the MMC senses that the hot-swap handle is secured and commences communication with the MCH, primarily relaying the module's FRU information and sensor data. Subsequently, the MCH authorizes the 12V payload power, fabric interface, and clock interface for the module, signaling the module's activation. Once the MMC and the system manager complete their interaction, the NATview [31] software can be employed. This software recognizes the AMC board, displays the entire chassis's status, and facilitates monitoring of various sensors, including hot-swap handles and temperature sensors. Through extensive testing, it was confirmed that the NES-RTOS-MMC effectively executed all the MMC's essential functions.

4.2 FPGA firmware design

The FPGA firmware was developed using Verilog. Fig. 3 shows the main block diagram of the FPGA code. An external trigger module was used to respond to the trigger signal and allow the system to start operating immediately. The FPGA memory stored the parameters for data processing and gain control.

Fig. 3 Main block diagram of FPGA code. The red arrows denote the data path inside FPGA.

The data path inside the FPGA is highlighted by a red arrow. Signals from the BC501A detector are digitized using an ADC with a 500 MSPS and 14-bit resolution. Configuration for these four ADCs is managed by the ADC Config module. Meanwhile, the CLK_{spl} control module orchestrates the LMK04828B clock conditioner chip to produce a 500 MHz ultra-low jitter clock for ADC sampling. Within this setup, the FPGA receives two simultaneous 14-bit samples at half the ADC's sampling clock rate, which is 250 MHz, employing the double data rate (DDR) format. To fetch data from both rising and falling clock edges, the input DDR (IDDR) register is utilized, which then transitions this data into a format suited for single-edge sampling. To facilitate transfer through a 32-bit channel, two 14-bit data inputs per clock cycle are consolidated into a single 32-bit word within a buffer.

The SAQP system operates in two primary modes: PSD and acquisition. Simultaneously, data from the buffer are funneled into two separate paths – the PSD mode and the acquisition mode within the data-processing module. Subsequently, based

on the operational mode, the data selection module handpicks the data and packages it into suitable formats for storage and display. Ultimately, data is transmitted to the host computer via a PCIe link for both storage and visual representation. Detailed descriptions of the PSD, acquisition, and data transfer modules are provided in subsequent sections.

4.2.1 PSD mode

The BC501A scintillator detector is sensitive to neutron and gamma radiations. Therefore, n-γ discrimination must be conducted to separate the neutron signal. Neutrons and gamma rays can be discriminated in a liquid scintillation detector because of the difference in the time decay constants of the signals induced by them, as shown in Fig. 4. Compared with gamma signals, neutron signals have longer decay times and tails. Therefore, n-γ discrimination can be performed via Pulse Shape Discrimination (PSD).
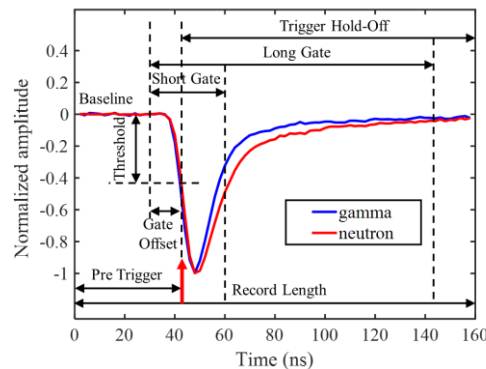
Fig. 4 Neutron and gamma-ray waveform from the BC501A detector recorded by SAQP system. The blue line is gamma-ray signal. The red line is neutron signal. The red arrow indicates the trigger position of the pulse. This figure also summarizes the PSD parameters. Long Gate, Short Gate, Gate Offset, Pre-Trigger, Trigger Hold-Off, and Record Length are shown for one pulse signal.

The pulse-related configuration parameters required by the PSD algorithm are shown in Fig. 4. The PSD algorithm performs a two-gate integration on the input pulse. For each pulse, the long-gate integral value Q_{LONG} and short-gate integral value Q_{SHORT}

were calculated starting from the left side of the Gate Offset. The ratio between the pulse tail integral and long gate integral provides the PSD factor for n-γ discrimination. The PSD factor of the neutron pulses was greater than that of the gamma pulses.

$$PSD = \frac{Q_{LONG} - Q_{SHORT}}{Q_{LONG}} \tag{1}$$

Fig. 5 presents a functional block diagram of the PSD algorithm. The algorithm consistently determines the baseline value based on a predetermined baseline length within the program. The input signal bifurcates into two channels: one undergoes comparison with the threshold value, with the trigger activated once the input signal surpasses this threshold. The other channel experiences a delay based on a set number of samples (pre-trigger), allowing for Q_{LONG} and Q_{SHORT} calculations to commence before the trigger's initiation. Throughout the gate integration phase, the baseline remains consistent with its most recent average value, which is later utilized to offset the baseline. To mitigate pulse pile-up events, the Trigger Hold-Off value is set in alignment with the signal width. Throughout the Trigger Hold-Off duration, the baseline remains frozen and other triggering signals are suppressed. Once the Trigger Hold-Off concludes, the FPGA prepares to process the upcoming pulse, subsequently transmitting the timestamp, Q_{LONG}, Q_{SHORT}, and the pulse peak of the previous pulse to the host computer.

The algorithm's dead time comprises the recorded length in addition to the baseline. Upon detecting a trigger event, the FPGA prioritizes sending the pulse waveform data to the host computer. It subsequently calculates the gate integral, restores the baseline, and concurrently sends Q_{LONG}, Q_{SHORT}, and the pulse peak values. As a result, the algorithm's theoretical count-rate limit is influenced by the pulse width.
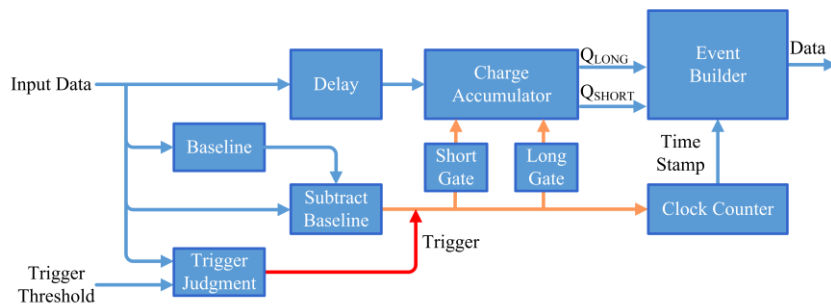

Fig. 5 Functional block diagram of the PSD algorithm.

4.2.2 Acquisition mode

The optimal length for the Baseline, Long Gate, Short Gate, and other parameters depicted in Fig. 4 are contingent upon the pulse's width and shape. Notably, the length of the long and short gates play a pivotal role in the n-γ discrimination performance. During system debugging, the Acquisition mode facilitates the configuration of PSD-mode parameters by visualizing the pulse waveform on a host computer. In this mode, a threshold is determined, and all events surpassing this amplitude (known as trigger events) are documented as pulse shapes accompanied by a timestamp. The length of the recorded event is the sum of Pre-trigger and Trigger hold-off. After the acquisition, the data undergoes offline processing.

4.2.3 Data transfer module

With a 500 MSPS at 14 bits resolution, the data volume for the four channels reached an impressive 3.3 GB/s. To mitigate the data throughput from the SAQP system to the host computer, the SAQP module only records the trigger events with predefined number of samples and a timestamp. An 80-sample pulse record length aptly processed the BC501A detector signals. As a result, the data volume needed to capture the entire pulse waveforms for the four channels was curtailed to 1 GB/s at a count rate of 2 Mcps. The x4-PCIe Gen2, boasting a theoretical bandwidth of 2 GB/s, was chosen as the communication protocol to bridge the SAQP system and the host computer [32]. In this research, a PCIe communication system was developed, leveraging the IP core and driver offered by Xillybus [33].

Xillybus provides a straightforward, user-friendly, DMA-based end-to-end turnkey solution for transferring data between an FPGA and a host operating on Linux or Windows. It incorporates both an FPGA IP core and a computer driver. Users can define the number of streams, their directions, and additional attributes, allowing for a tailored balance between bandwidth performance, synchronization and design simplicity [34]. In an FPGA, the user application logic interfaces with the Xillybus IP

core, employing either FIFO or synchronous memory as intermediaries, as depicted in Fig. 3. In this setup, the FIFO serves as a data buffer between the user application logic and the Xillybus IP core, safeguarding against data loss. The Xillybus IP core and its driver seamlessly stream data between the FPGA's FIFOs and the corresponding device files on a computer. Through these device files, the computer application retrieves data from the FPGA.

In this design, the data transfer module encompasses seven data streams: four data transfer channels each 32 bits wide, a 64-bit display channel, a trigger channel, and a memory channel. The four 32-bit data transfer channels are designated to relay their respective ADC data. Importantly, the data processing and transfer functionalities for these four ADC channels operate independently. This independence allows for the adjustment of different operational parameters, facilitating the simultaneous acquisition of data from detectors with varying signal widths. The display channel's primary role is to convey data to a computer for real-time visualization. Given this real-time requirement, it is vital to minimize the data volume in the display channel. When in PSD mode, only the Q_{LONG}, Q_{SHORT}, and pulse peaks are compiled into a 64-bit word, which is then transmitted to a computer via the display channel. However, in Acquisition mode, the display channel relays only a single pulse waveform of data within a configurable time span. The trigger channel, on the other hand, is integral in responding to trigger signals, ensuring all four channels initiate operations in unison. Within the FPGA, a dedicated memory houses parameters essential for data processing and gain control. Users can modify these stored parameters through the computer application by writing to the associated device files. It's noteworthy that, due to the 8b/10b encoding overhead in the PCIe Gen2's physical layer protocol, the SAQP system's real bandwidth settles at 1.6 GB/s.

5 Experimental results and discussion

Initially, the SAQP system were assessed using a signal generator in conjunction with the FFT methodology. The four channels displayed an Effective Number of Bits

(ENOB) close to 11.2 bits, with noise registering under 1 mV. Following this, both radioactive source and EAST experiments were undertaken to gauge the SAQP system's efficacy. The radioactive source experiment specifically aimed at assessing the SAQP system's capacity for n-γ discrimination. Meanwhile, the EAST experiment was designed to validate the integrated capabilities of SAQP system, ensuring the system align with the stipulations of the NES system.

5.1 Radioactive source experiment

The n-γ discrimination performance experiments was performed with ^{252}Cf neutron source and EJ301 scintillator detector, which has the same chemical composition and performance as the BC501A detector. However, EJ301 scintillator detector is manufactured by a different vendor. The ^{252}Cf neutron source is typically employed to produce neutrons. Along with this, gamma rays emerge from the α-decay and the fission byproducts. Notably, the energy range of neutrons emanating from the ^{252}Cf source predominantly falls between 1 and 8 MeV [35], which is similar to the energy range of deuterium-deuterium (DD) fusion neutrons. Therefore, it is suitable for evaluating the n-γ discrimination performance of SAQP system for detecting the fusion neutrons. A two-dimensional plot of the PSD factor versus pulse height is shown in Fig. 6(a), where the color scale indicates the number of events corresponding to a given PSD factor and pulse height set. A clear separation can be observed in Fig. 6(a), where the neutron events are located above a PSD factor of 0.1. Figure of Merit (FOM) is used to evaluate the n-γ discrimination performance of the system. The FOM at a given pulse height is evaluated from Fig. 6(b) using the formula Sn/(FWHMn + FWHMγ), where Sn denotes the separation between the centroids of the n and γ distributions while FWHMn and FWHMγ denote their full widths half maximum.
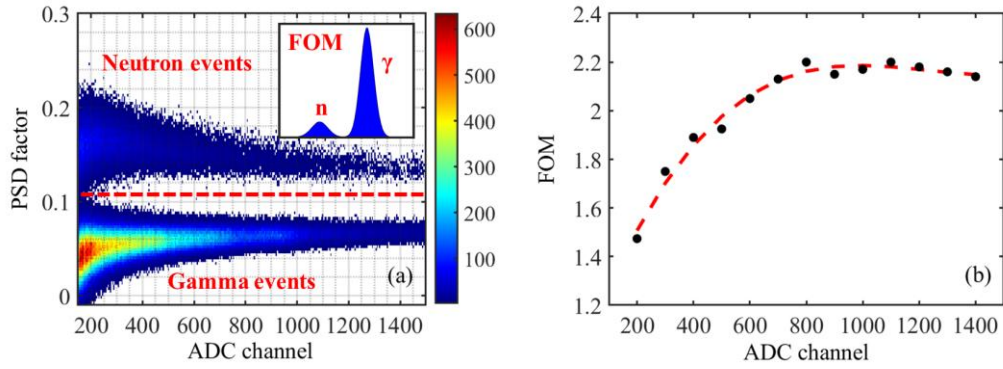
Fig. 6 (a) Two-dimensional plot of PSD factor versus pulse height from EJ301 detector using ^{252}Cf as neutron source. The color scale is used to indicate the number of events corresponding to a given PSD factor, pulse height set. The neutron and gamma-ray events are separated by the red dashed line, where the PSD factor is 0.1. (b) FOM versus pulse height.

5.2 EAST experiment

In an effort to evaluate the integrated capabilities of the SAQP systems, the SAQP setup, equipped with a BC501A detector, functioned as a neutron spectrometer to measure neutrons in deuterium plasma during the EAST experiment in June 2022.

Data from shot No.112880, which marked the highest neutron yield in the recent set of EAST experiments, were selected for a qualitative assessment of the SAQP system's n-γ discrimination capability at elevated count rates. Fig. 7 depicts the progression of the fundamental plasma parameters from shot No.112880, captured with a time resolution of 10 ms. Within this shot, key parameters included a plasma current (Ip) of approximately 400 kA and a central electron density (ne) of approximately 5×10^{19} m^{-3} during its flattop phase. Additionally, four NBI beamlines, all powered at 1.7 MW, began their injection into the plasma at varied intervals but concluded synchronously within shot No.112880.
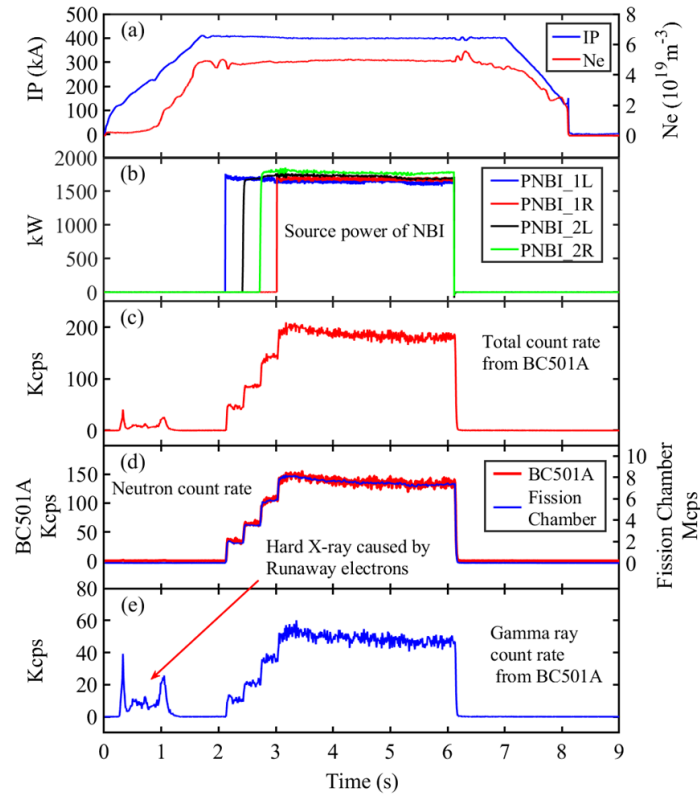
Fig. 7 The time evolutions of fundamental plasma parameters from shot No.112880, captured at a 10-ms resolution. (a) Evolution of plasma current and central electron density over time. (b) Change in beamline power for NBI-1L, NBI-1R, NBI-2L, and NBI-2R over time. (c) Fluctuation of the total count rate as captured by the BC501A detector. (d) Tracking of neutron emissions as recorded by the BC501A detector and ^{235}U fission chamber. (e) Variations in the gamma-ray count rate as documented by the BC501A detector.

In shot No.112880, the SAQP system executed real-time n-γ discrimination while capturing the entire pulse waveform. Fig 7(c) illustrates the time evolution of the total count rate as detected by the BC501A using the SAQP system. With the injection of NBI into the plasma, there was a significant production of neutron and gamma-ray emissions from 2.1 to 6.1 s. As the four NBI beamlines were injected concurrently into the plasma, the count rate of the NES system peaked at 200 kcps.

In Fig. 8(a), a two-dimensional representation contrasts the PSD factor against the pulse height from the BC501A detector for shot No.112880, while Fig. 8(b) presents the FOM for a specific pulse height. Contrary to controlled lab conditions, the BC501A detector is situated in the EAST Hall, exposed to substantial electromagnetic

interference during EAST discharges. Furthermore, the detector signal needs to traverse through extensive lengths of shielded cable, spanning tens of meters, to reach the neutron diagnostic laboratory before acquisition by the SAQP system. This transit can lead to amplified noise, potential signal distortions, and may hinder the n-γ discrimination capability. As depicted in Figs. 8(b) and 6(b), the FOM from the EAST experiment is somewhat diminished compared to the radioactive source experiment, though a distinct separation is evident in Fig. 8(a). Specifically, regions above a PSD factor of 0.2, demarcated by the red dotted boundary, indicate neutron events. A notable distinction from the radioactive source test is the presence of pile-up events in the EAST experiment, a result of its high count rate. To address these pile-up events, two strategies can be employed: adjusting the pulse record length to diminish the likelihood of such events, or employing a two-dimensional representation for their removal. Fig. 8(d) showcases a typical waveform for a pile-up pulse. These pile-up pulses exhibit a greater PSD factor, causing them to appear as outliers situated above the neutron events. The sporadic points encircled by the black dotted line in Fig. 8(a) correspond to these pile-up occurrences. The neutron pulse-height spectrum is portrayed in Fig. 8(c). Typically, EAST, operating on deuterium plasma, predominantly yields 2.45 MeV DD fusion neutrons during standard discharges [36]. A recoil proton edge emerges in the neutron pulse-height spectrum due to the energy deposition by these 2.45 MeV neutrons in the detector, as signified by the red arrow in Fig. 8(c).
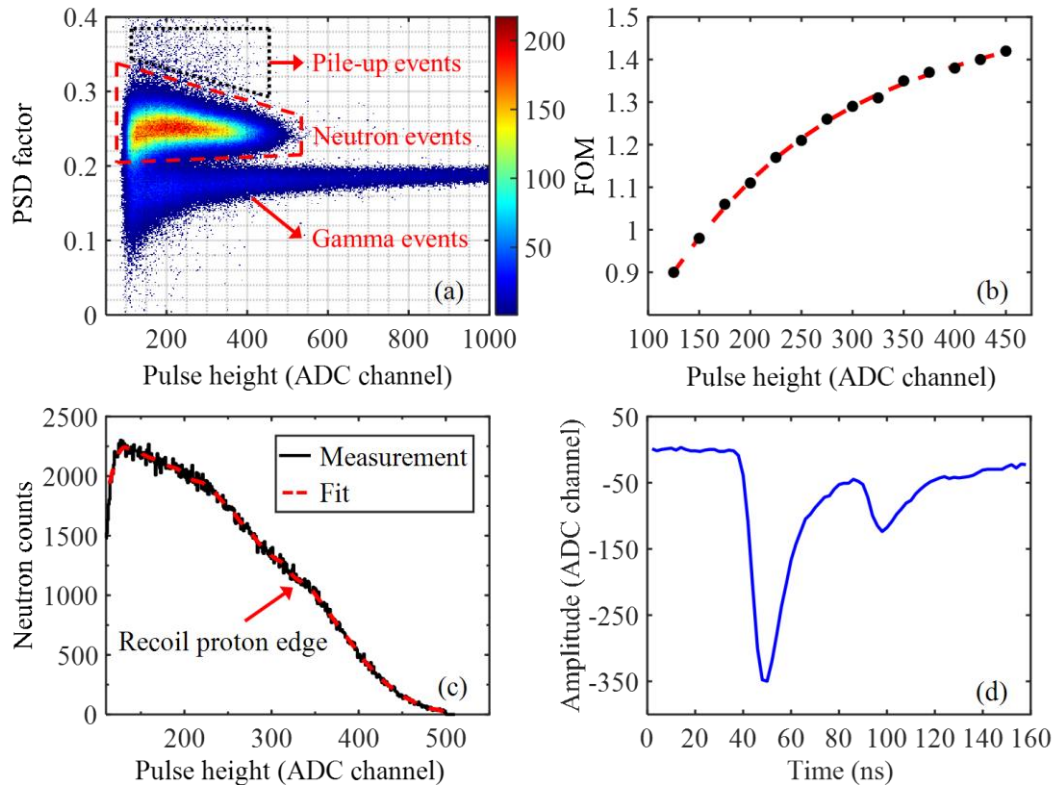
Fig. 8 (a) Two-dimensional plot of PSD factor versus pulse height from BC501A detector (shot No.112880). (b) FOM versus pulse height. (c) Neutron signal pulse height spectrum. (d) Pulse waveform of a typical pile-up pulse recorded by SAQP system.

Following the separation of neutron and gamma signals, Fig. 7(d) and 7(e) display the time evolutions of the neutron and gamma count rates, respectively. The time-evolving neutron count rate captured by the BC501A detector is juxtaposed with data from a ^{235}U fission chamber. While the ^{235}U fission chamber is sensitive to gamma radiation, neutrons and gamma rays occupy distinct amplitude ranges, with the gamma signal amplitude being relatively subdued. For the ^{235}U fission chamber system, an appropriate pulse amplitude discrimination threshold was established to minimize the impact of gamma radiation. Thus, the ^{235}U fission chamber can provide precise measurements of neutron flux [37]. Fig. 7(d) shows that the time evolution of the neutron count rate from the BC501A detector is consistent with the data from the ^{235}U fission chamber and is closely related to the time dependence of the NBI power. Runaway electrons are generated during the start-up phase of the discharge [10]. In this phase, the BC501A signal detected bremsstrahlung emission in the hard X-ray range produced by runaway electrons. Consequently, during the discharge's start-up phase, a

distinct peak appears in the time evolution of the gamma count rate. This contrasts with the time evolution of the neutron count rate, as depicted in Fig. 7(d) and 7(e). This observation demonstrates the capability of distinguishing between neutron and gamma events.

To further validate the n-γ discrimination performance of the SAQP system, Fig. 9 presents a comparison between the total neutron counts during each discharge as captured by the BC501A detector and those recorded by the ^{235}U fission chamber. Each data point symbolizes an individual NBI heating shot ranging from No.112653 to NO.112973. A strong linear relationship is evident between the two datasets, with a correlation coefficient R^2 of 0.9992. The close alignment between these datasets reaffirms the accuracy of the data processed by the SAQP system.
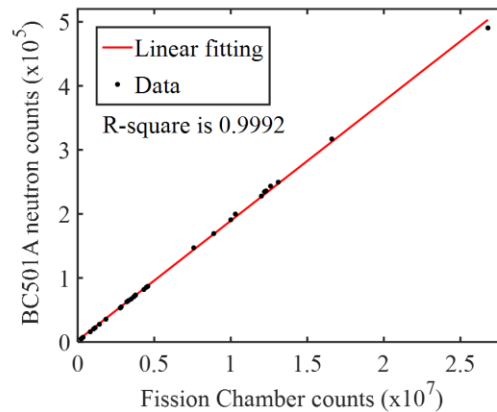
Fig. 9 Neutron counts measured by the BC501A detector versus the one measured by ^{235}U fission chamber, and each point represents an individual discharge.

The n-γ discrimination algorithm, grounded in the two-gate integral method, effectively discerns neutron events from gamma and pile-up pulse events, validating the data from the SAQP system.

During the start-up phase of the discharge, especially when plasma confinement is suboptimal, there is a surge in hard X-ray emissions due to runaway electrons. This surge elevates the count rate for the NES system. Although an increase in the count rate from gamma rays is not the concern of the NES system, an abrupt spike risks saturating the PSD algorithm and transfer bandwidth, potentially leading to data loss.

Considering the pulse width, the pulse record length was configured at 160 ns, and the baseline at 24 ns. This setup mandates 184 ns for the algorithm to process a single pulse. In theory, the PSD algorithm can handle up to five million pulse events per second. Although the bandwidth can manage data transfer from one channel at a count rate of 5 Mcps, the NES system seldom reaches such high count rates, since numerous pile-up events could compromise n-γ discrimination and pulse height analysis.

For shot No.114644, a total count rate reaching 4 Mcps was confirmed. Fig. 10(a) depicts the time evolution of Hard X-ray intensity as captured by the runaway electron diagnostic system, whereas Fig. 10(b) reveals the temporal progression of the BC501A detector's total count rate. During the start-up phase (from 0.8 s to 1.7 s) of discharge No.114644, a significant number of runaway electrons led to intense hard X-ray emissions, resulting in a substantial spike in the BC501A detector's count rate, peaking at 4 Mcps. The entire pulse waveform, captured during the peak count rate for shot No.114644, is showcased in Fig. 10(b). This substantiates that the SAQP system is capable of logging a full pulse waveform even when the NES system's count rate hits 4 Mcps.
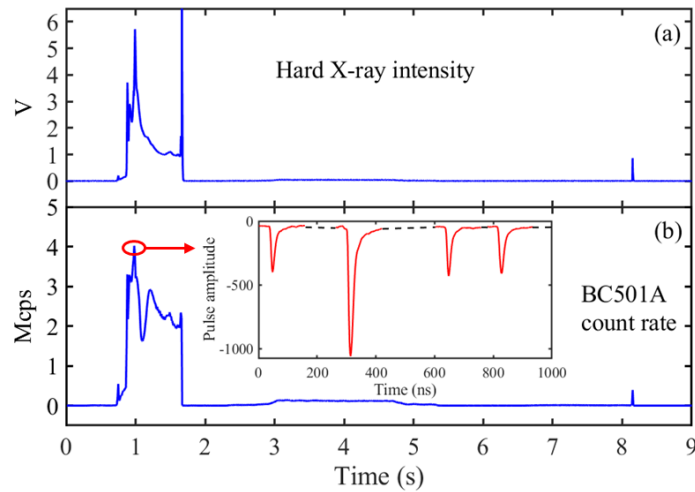

Fig. 10 (a) The time evolution of Hard X-ray intensity from the runaway electron diagnostic system. (b) The time evolution of total count rate from BC501A detector with the time resolution of 10 ms. The entire pulse waveform recorded at the highest count rate of shot No.114644 is also shown this figure.

6 Conclusion

In this study, a high-speed digital pulse signal acquisition and processing system was developed for the NES system on EAST using the MTCA architecture. This marked the first application of the MTCA framework in the EAST diagnostic system. The four input channels of the system demonstrated an ENOB of approximately 11.2 bits, with noise levels not exceeding 1 mV. This ensures compatibility with the projected signal-to-noise ratio of the input pulses. Achieving a bandwidth of 1.6 GB/s in PCIe DMA mode, the SAQP system's real-time n-γ discrimination algorithm, with its single pulse processing duration of 184 ns, effectively differentiates the n-γ signal. Under the conditions of EAST experiments, the FOM reaches 1.4. Therefore, the advanced SAQP system ensures that the NES system is tailored for high-parameter experiments. It can accommodate a high count rate of up to 2 Mcps, perform real-time n-γ discrimination algorithms, and consistently record the entire pulse waveform without data loss.

Acknowledgments

Author contributions

All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by Yong-Qiang Zhang, Li-Qun Hu, Guo-Qiang Zhong, Hong-Rui Cao, Jin-Long Zhao, Li Yang and Qiang Li. The first draft of the manuscript was written by Yong-Qiang Zhang, and all authors commented on previous versions of the manuscript. All the authors read and approved the final version

of the manuscript.

Data Availability Statement

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